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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/561,089	12/16/2005	Yoshihiro Hayashi	201558-9001	2457

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MICHAEL BEST & FRIEDRICH LLP
Two Prudential Plaza
180 North Stetson Avenue, Suite 2000
CHICAGO, IL 60601

EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/561,089	HAYASHI ET AL.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *38-77* is/are pending in the application.

4a) Of the above claim(s) *67-70 and 75-77* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *38-47,52-60,64-66,73 and 74* is/are rejected.

7)☒ Claim(s) *48-51 and 61-63 and 71-72* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/27/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 38-66 and 71-74 in the reply filed on 04/22/09 is acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 43 recites the limitation "said low permittivity substrate region" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 73 recites the limitation "said low-permittivity insulator rods" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 74 recites the limitation "said low-permittivity insulator rods" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 38, 40, 41, 42, 53, 54, 56, 64, 65, and 66 are rejected under 35 U.S.C. 102(b) as being anticipated by Japan 2001308273.

With respect to claim 38, Japan '273 teaches a semiconductor device comprising a semiconductor substrate 51having therein a low-capacitance substrate region (11) (note that the presence of the plurality of insulating columns would inherently result in a low capacitance substrate), a transistor Q11 formed on a surface area of said semiconductor substrate, and a multi-layered interconnection structure CP1, WL, CP,

S1 including a plurality of interlevel dielectric films 4,5 and a plurality of interconnect layers overlying said transistor, wherein: a plurality of substrate openings 11 are formed in said low-capacitance substrate region, penetrating at least an undermost one of said interlevel dielectric films to reach an internal of said semiconductor substrate. See all figures and English abstract and machine translation.

With respect to claim 40, Japan '273 further teaches wherein a length of said substrate openings within said semiconductor substrate is equal to or larger than halt" a thickness of said semiconductor substrate, or said substrate opening penetrate said semiconductor substrate.

With respect to claim 41, Japan '273 further teaches wherein said substrate openings are randomly arranged as viewed normal to a surface of said substrate. See fig. 4.

With respect to claim 42, since Japan '273 teaches said substrate openings are randomly arranged as viewed normal to a surface of said substrate, said substrate openings inherently are formed so that no linear current path is formed crossing said low- permittivity substrate region as viewed normal to a surface of said substrate.

With respect to claim 38, Japan '273 further teaches an inductor S1 is formed to overlie said low-permittivity substrate region. See fig. 1.

With respect to claim 54, Japan '273 further teaches an analog circuit S1 is formed on said semiconductor substrate in said low-capacitance substrate region.

With respect to claim 56, Japan '273 further teaches a logic circuit Q11 is formed on said semiconductor substrate in an area other than an area in which said low-capacitance substrate region is formed.

With respect to claim 57, Japan '273 further teaches a logic circuit Q11 is formed on said semiconductor substrate in an area other than an area in which said high-permeability region is formed.

With respect to claim 64, Japan '273 further teaches an interconnect configured by a plurality of interconnect layers is provided in said low-capacitance substrate region.

With respect to claim 65, Japan '273 further teaches said interconnect layers configure an inductor.

With respect to claim 66, Japan '273 further teaches interconnects in said plurality of interconnect layers are connected electrically in parallel through a plurality of via-plugs.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Japan 2001308273 as applied to claims 38, 40, 41, 42, 53, 54, 56, 64, 65, and 66 above, and further in view of Srinivasan et al. (US pub 20040185183).

With respect to claim 39, Japan '273 teaches that the openings are filled with insulating material but fail to teach the insulating material has low permittivity or SiOF or silicon oxide with added fluorine.

Srinivasan et al. teach adding fluorine to a silicon oxide of an insulating material to reduce a flow temperature of the material. See para [0014].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Srinivasan et al. to achieve the above benefit.

Claims 43, 44, 73, and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Japan 2001308273 as applied to claims 38, 40, 41, 42, 53, 54, 56, 64, 65, and 66 above, and further in view of Onuma et al. (US pub 20020050626).

With respect to claim 43, Japan '273 fails to teach that a high-permeability region is provided over said low-permittivity substrate region or a substrate region, said high-permeability region including a high-permeability material embedded in an interlevel dielectric film.

Onuma et al. teach an integrated inductor in which a high-permeability region 16 is provided over a substrate region, said high- permeability region including a high-permeability material embedded in an interlevel dielectric film 14 or 18 to improve the inductance value. See fig. 1B and associated text, particularly, para [0046].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Onuma et al. to achieve the above benefit.

With respect to claim 43, Onuma et al. further teach said high-permeability region includes therein a high-permeability magnetic rod arranged and including said high-permeability material having an electric conductivity and embedded in respective film opening having an aspect ratio (ratio of depth to diameter or length of a side) of 1 or above, said film opening penetrating at least one of said interlevel dielectric films to reach another of said interlevel dielectric films.

Onuma et al. teach forming only one high-permeability magnetic rod but fail to teach forming a more than one high-permeability magnetic rod.

However, given the teaching the presence of a high-permeability magnetic rod over a substrate region would improve the inductance value, It would have been obvious to one of ordinary skill in the art of making semiconductor devices add more than one rod to achieve additional improvement in inductance value.

With respect to claim 44, Onuma et al. as described above further teach said high-permeability region includes therein a plurality of high-permeability magnetic rods arranged and including said high-permeability material having an insulating property and embedded in respective film openings, said film openings penetrating at least one of said interlevel dielectric films to reach another of said interlevel dielectric films. See claims of Onuma et al.

With respect to claim 73, Japan '273 in combination with Onuma et al. further teaches said low-permittivity insulator rods have a topmost surface located lower than a topmost surface of contact plugs CP1 in said low-capacitance substrate region.

With respect to claim 74, Japan '273 in combination with Onuma et al. further teaches an insulating film (the layer above the region 11) is disposed to cover said low-permittivity insulator rods, said insulating film having a higher permittivity and higher mechanical strength than another insulating film embedded in said rods (since insulating film embedded in the rods are made of SiOF).

Claims 58, 59, and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Japan 2001308273 as applied to claims 38, 40, 41, 42, 53, 54, 56, 64, 65, and 66 above, and further in view of Masaki (US pub 20010053672).

With respect to claim 58, Japan '273 fails to teach forming a on-chip antenna interconnect on the substrate.

Masaki teaches forming a on-chip antenna interconnect 1 on a substrate to achieve a broader band characterisic. See 1A and associated text and abstract.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Masaki to achieve the above benefit.

With respect to claim 59, Masaki further teaches said on-chip antenna interconnect is formed in a peripheral area of a semiconductor chip.

With respect to claim 60, Masaki further teaches said on-chip antenna interconnect is formed in L-character. See paras [0036] and [0071].

Claims 46, 47, 53, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Japan 2001308273 in combination with Onuma et al. (US pub 20020050626).

With respect to claim 46, Japan '273 teaches as emiconductor device comprising a semiconductor substrate 51, a transistor Q11 formed on a surface area of said semiconductor substrate, and a multi-layered interconnection structure CP1, WL, CP, S1 including a plurality of interlevel dielectric films 4,5 and a plurality of interconnect

layers overlying said transistor. See all figures and English abstract and machine translation.

Japan '273 fails to teach a high-permeability region is provided in an interlevel dielectric film, wherein said high-permeability region includes therein a plurality of high-permeability magnetic rods including a high-permeability material embedded in respective film openings, said film openings having an aspect ratio (depth/diameter or a side) of 1 or above and penetrating at least one of said interlevel dielectric films to reach another of said interlevel dielectric films.

Onuma et al. teach an integrated inductor in which a high-permeability region is provided in an interlevel dielectric film 14 or 18, wherein: said high-permeability region includes therein a high-permeability magnetic rod including a high-permeability material embedded in respective film openings, said film openings having an aspect ratio (depth/diameter or a side) of 1 or above and penetrating at least one of said interlevel dielectric films to reach another of said interlevel dielectric films to improve the inductance value. See fig. 1B and associated text, particularly, para [0046].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Onuma et al. to achieve the above benefit.

Further with respect to claim 46, Onuma et al. teach forming only one high-permeability magnetic rod but fail to teach forming a more than one high-permeability magnetic rod.

However, given the teaching the presence of a high-permeability magnetic rod over a substrate region would improve the inductance value, It would have been obvious to one of ordinary skill in the art of making semiconductor devices add more than one rod to achieve additional improvement in inductance value.

With respect to claim 47, Onuma et al. further teach said high-permeability material has either an electric conductivity or an insulating property. See claims of Onuma et al.

With respect to claim 53, Japan '273 further teaches an inductor S1 is formed to overlie said low-permittivity substrate region. See fig. 1.

With respect to claim 54, Japan '273 further teaches an analog circuit S1 is formed on said semiconductor substrate in an area including said high- permeability region.

Allowable Subject Matter

Claims 48, 49, 50, 51, 61-63, 71-72 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

/Long Pham/
Primary Examiner, Art Unit 2814